example, an analog-to-digital converter, or a communication circuit such as an Ethernet PHY. OPAMP **202** comprises first differential stage **204** and a final output stage comprising nMOSFET **206** biased by current source **210**, where the output signal is taken at output port **212** and input signals are applied at input ports **214** and **216**. Miller compensation is applied to nMOSFET **206** by connecting capacitor **208** as shown in Fig. 2. Other stages, employing nMOSFETs, pMOSFETs, or both types of transistors, may be present in OPAMP **202**, but for simplicity are not shown. The voltage difference between terminals **218** and **220** of capacitor **208** may be small, such as much less than 0.1 volts.

In the Claims

Please cancel without prejudice claims 2-8 and 18-20.

Please amend claims 1 and 17 to read as provided below.

Please add new claims 21 and 22 as provided below.

For convenience, all presently active claims are provided below.

1. (Amended) A device comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a gate, source, and drain;

wherein bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

9. A device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a third field effect transistor having a gate, source, and drain, wherein the sources and drains of the first and second field effect transistors and the drain and gate of the third field effect transistor are all connected to each other.

10. The device as set forth in claim 9, wherein an impedance between the gates of the first and second field effect transistors is substantially capacitive.

11. A device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a bipolar transistor having a base, emitter, and collector, wherein the sources and drains of the first and second field effect transistors and the base and collector of the bipolar transistor are all connected to each other.

12. The device as set forth in claim 11, wherein an impedance between the gates of the first and second field effect transistors is substantially capacitive.

13. An amplifier comprising:

an output stage having an output port and an input port; and

a device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a third field effect transistor having a gate, source, and drain, wherein the sources and drains of the first and second field effect transistors and the drain and gate of the third field effect transistor are all connected to each other;

wherein the gate of the first field effect transistor is connected to the output port and the gate of the second field effect transistor is connected to the input port.

14. The device as set forth in claim 13, wherein the output stage comprises a field effect transistor having a gate and a drain, wherein the gate of the output stage is connected to the input port and the drain of the output stage is connected to the output port.

15. An amplifier comprising:

an output stage having an output port and an input port; and

a device comprising:

a first field effect transistor having a gate, source, and drain;

a second field effect transistor having a gate, source, and drain; and

a bipolar transistor having a base, emitter, and collector, wherein the sources and drains of the first and second field effect transistors and the base and collector of the bipolar transistor are all connected to each other;

wherein the gate of the first field effect transistor is connected to the output port and the gate of the second field effect transistor is connected to the input port.

16. The device as set forth in claim 15, wherein the output stage comprises a field effect transistor having a gate and a drain, wherein the gate of the output stage is connected to the input port and the drain of the output stage is connected to the output port.

17. (Amended) A communication circuit comprising:

an amplifier comprising a capacitor to provide compensation, the capacitor comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a gate, source, and drain;

wherein bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the gate and drain of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.

21. (New) A device comprising:

a first field effect transistor having a gate, a source, and a drain;

a second field effect transistor having a gate, a source, and a drain; and

a bias transistor having a base, emitter, and collector;

wherein bias transistor and the first and second field effect transistors are coupled to each other so that the sources and drains of the first and second field effect transistors and the base and collector of the bias transistor have a substantially same voltage potential, and the bias transistor has substantially zero DC bias current.